

CLAIMS

What is claimed is:

1. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:
 - 5 growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;
 - lowering said acceptor-doped layer to a second temperature significantly lower
 10 than said first temperature during a cool-down process;
 - causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3 \times 10^{15} \text{ cm}^{-3}$ and $1 \times 10^{18} \text{ cm}^{-3}$, after said cool-down process; and
 15 annealing said p-type layer at a temperature below 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.
 2. The method of Claim 1 wherein said causing said acceptor-doped layer to be a p-type layer prior to annealing comprises substantially preventing additional hydrogen from diffusing into said acceptor-doped layer during said cooling process.
 - 20 3. The method of Claim 2 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.
 4. The method of Claim 2 wherein said preventing additional hydrogen from
 25 diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.
 5. The method of Claim 1 wherein said causing said acceptor-doped layer to be a p-type layer prior to said annealing comprises treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3 \times 10^{15} \text{ cm}^{-3}$.

6. The method of Claim 5 wherein said treating said surface comprises chemically etching said surface.
7. The method of Claim 5 wherein said treating said surface comprises plasma etching said surface.
- 5 8. The method of Claim 5 wherein said treating said surface comprises plasma cleaning said surface.
9. The method of Claim 5 wherein said treating said surface comprises chemically cleaning said surface.
- 10 10. The method of Claim 9 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_4OH .
11. The method of Claim 5 wherein said treating said surface comprises ultrasonically cleaning said surface.
12. The method of Claim 5 wherein said treating said surface comprises irradiating said surface with an electron-beam.
- 15 13. The method of Claim 5 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.
14. The method of Claim 1 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.
- 20 15. The method of Claim 1 wherein, after said cool-down process, said hole density is greater than $3 \times 10^{16} \text{cm}^{-3}$.
16. The method of Claim 1 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than $5 \times 10^{18} \text{cm}^{-3}$.

17. The method of Claim 1 wherein said annealing is carried out at a temperature in the range of 100-625°C.
18. The method of Claim 1 wherein said annealing is carried out at a temperature below 400°C.
19. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.
20. The method of Claim 1 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.
21. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.
22. The method of Claim 21 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.
23. The method of Claim 1 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.
24. The method of Claim 1 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.
25. The method of Claim 1 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.
26. The method of Claim 1 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.
27. The method of Claim 1 wherein said acceptor impurities comprise magnesium.

28. The method of Claim 1 wherein said annealing is carried out in a gas environment containing N_2 .
29. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 5000 ohm-cm.
- 5 30. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.